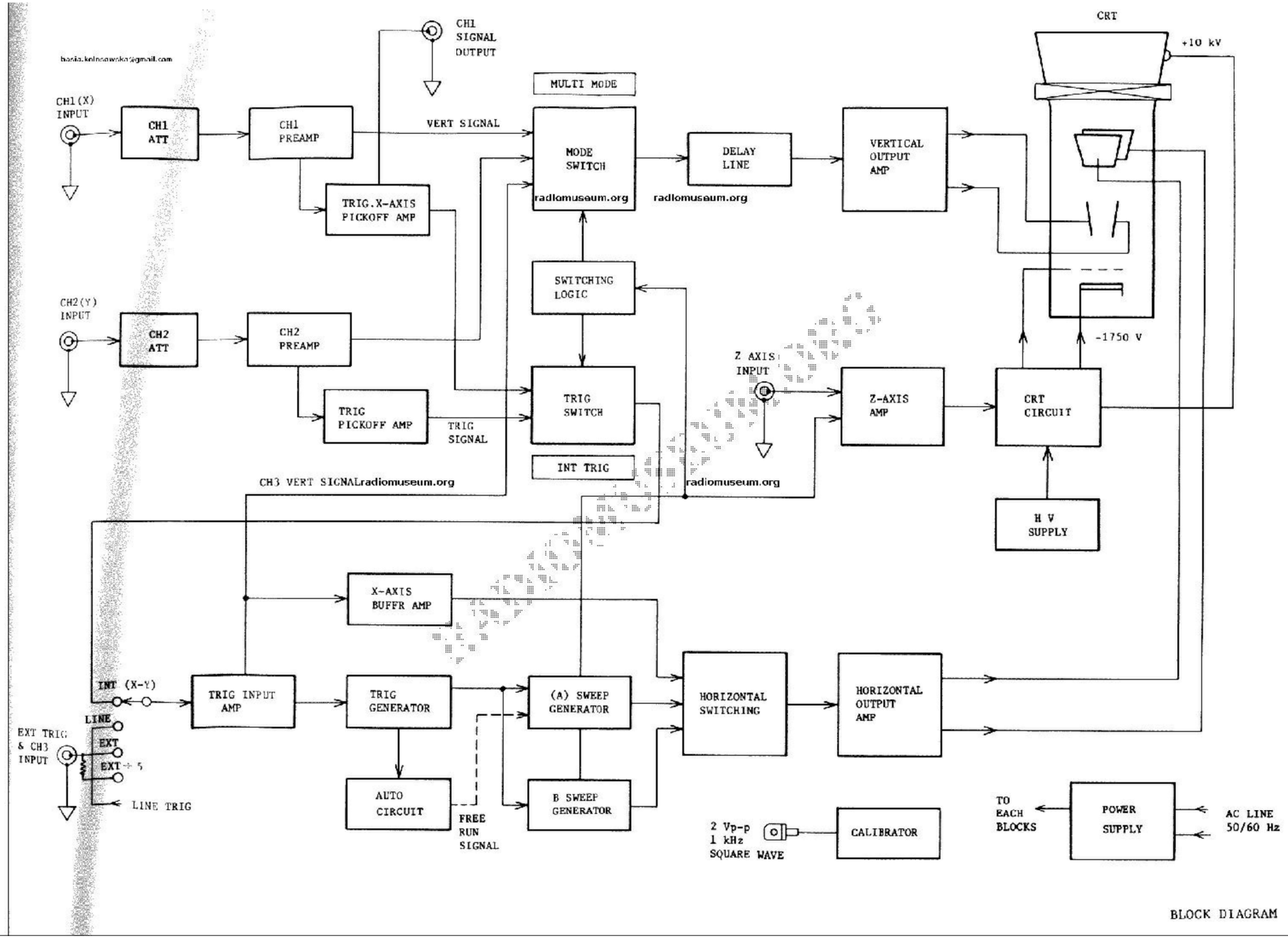
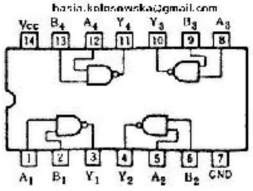
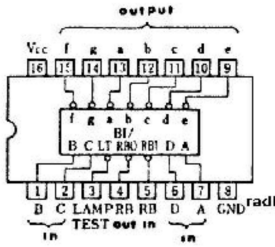

CH1 SIGNAL OUTPUT
CH1(X) INPUT
CH1 ATT
CH1 PREAMP
VERT SIGNAL
MULTI MODE
MODE SWITCH
DELAY LINE
VERTICAL OUTPUT AMP
CRT
+10 kV
TRIG.X-AXIS PICKOFF AMP
radiomuseum.org
CH2(Y) INPUT
CH2 ATT
CH2 PREAMP
SWITCHING LOGIC
-1750 V
Z AXIS INPUT
TRIG PICKOFF AMP
TRIG SIGNAL
TRIG SWITCH
Z-AXIS AMP
CRT CIRCUIT
INT TRIG
CH3 VERT SIGNALradiomuseum.org
H V SUPPLY
X-AXIS BUFFR AMP
INT (X-Y)
TRIG INPUT AMP
TRIG GENERATOR
(A) SWEEP GENERATOR
HORIZONTAL SWITCHING
HORIZONTAL OUTPUT AMP
LINE
EXT TRIG & CH3 INPUT
EXT
EXT ÷ 5
LINE TRIG
AUTO CIRCUIT
FREE RUN SIGNAL
B SWEEP GENERATOR
2 Vp-p 1 kHz SQUARE WAVE
CALIBRATOR
TO EACH BLOCKS
POWER SUPPLY
AC LINE 50/60 Hz
BLOCK DIAGRAM

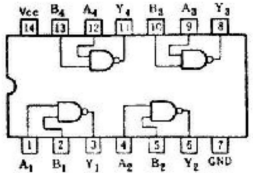
DIGITAL & ANALOG ICs



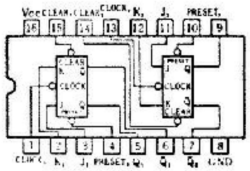
(TOP VIEW)
TC4011BP



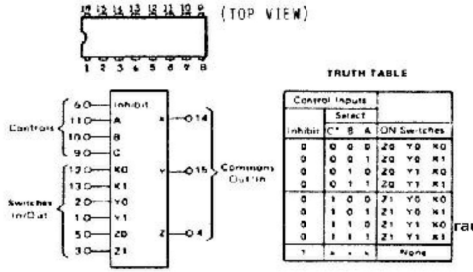
(TOP VIEW)
SN74LS47N



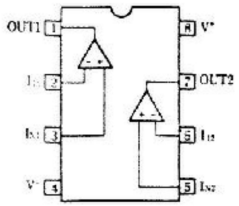
(TOP VIEW)
SN74LS00N
74F00PC



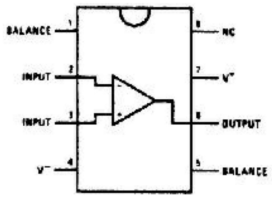
(TOP VIEW)
SN74S112N
SN74LS112N



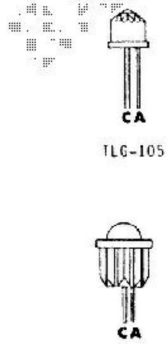
TC4053BP



(TOP VIEW)
μPC4558C



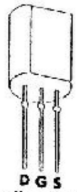
(TOP VIEW)
LF13741N
TL081CP



TLG-105

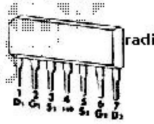
TLG102KN
TLR102KN

FET



2SK107-3
2SK117-BL
2SK170-V

2SK228



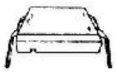
μPA68H

DIODE

GHV-06SSN

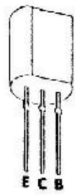
1S1588

1SS83 RD5.6JB
1SS86 RD6.8JB
HZ28 RD13JB
HZ36

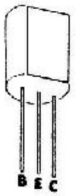


1G4B42

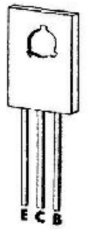
TRANSISTOR



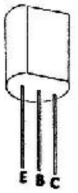
2SA844-D
2SC1907



2SC2570



2SA1144-O
2SB648A
2SC1846
2SD668A

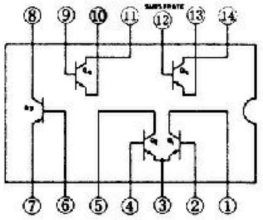


2SA1206-L

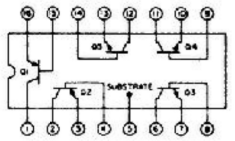
2SB834-Y
2SB861-C
2SD880-Y

2SA838-B
2SA1005-L
2SA1015-Y
2SC945-Q
2SC1843-E
2SC1885-R

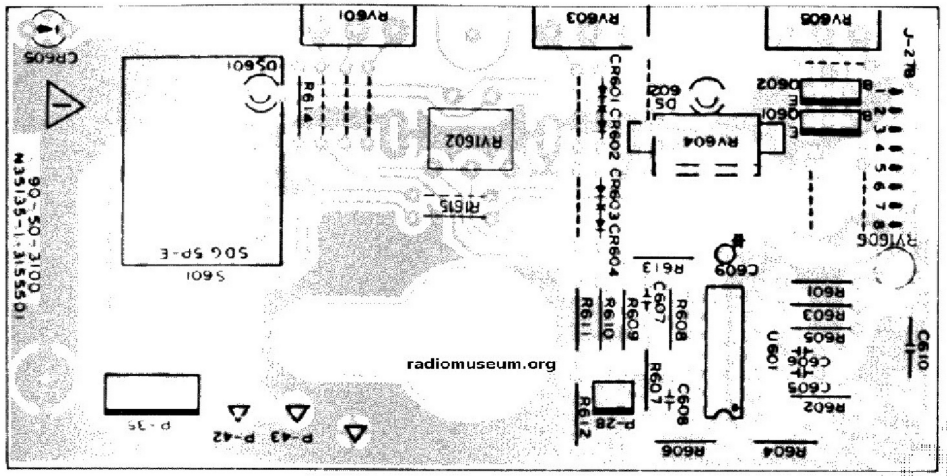
TRANSISTOR ARRAY



CA3086

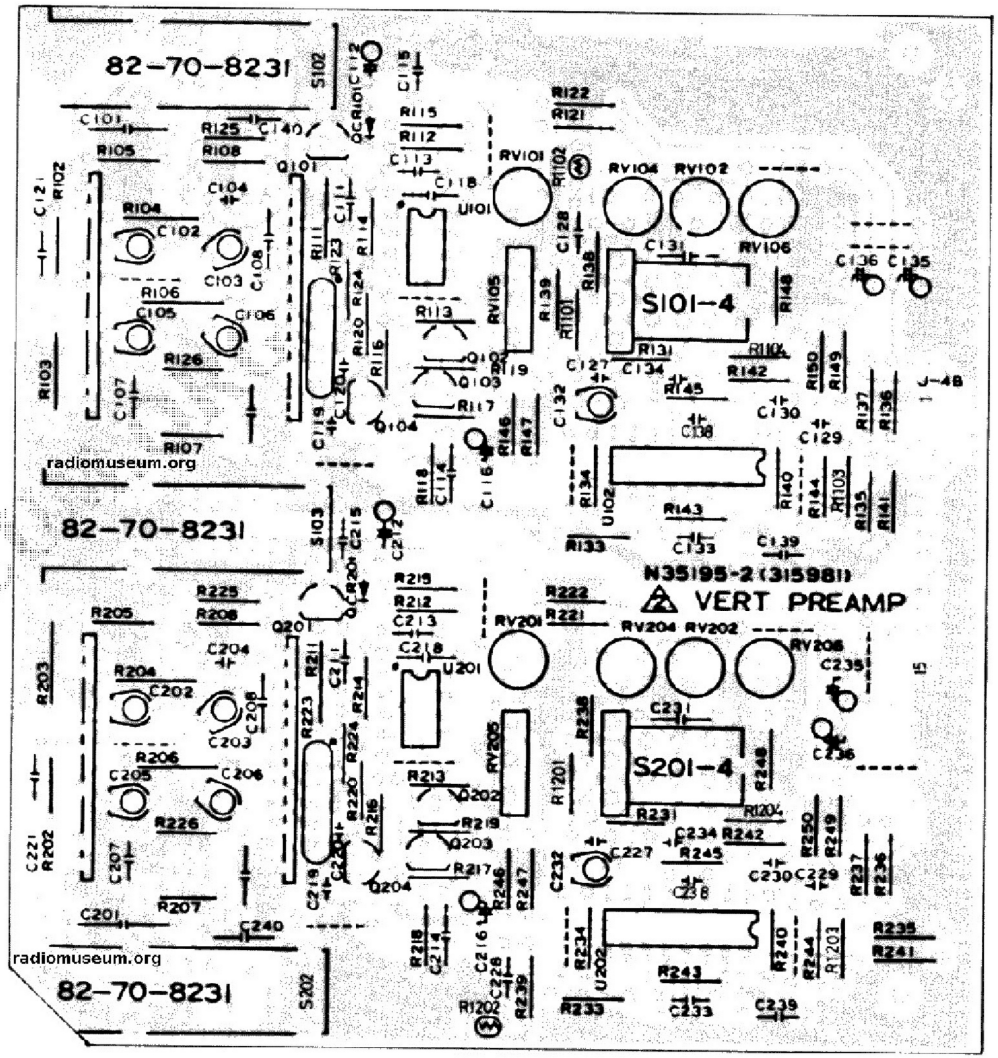


(TOP VIEW)
CA3127E



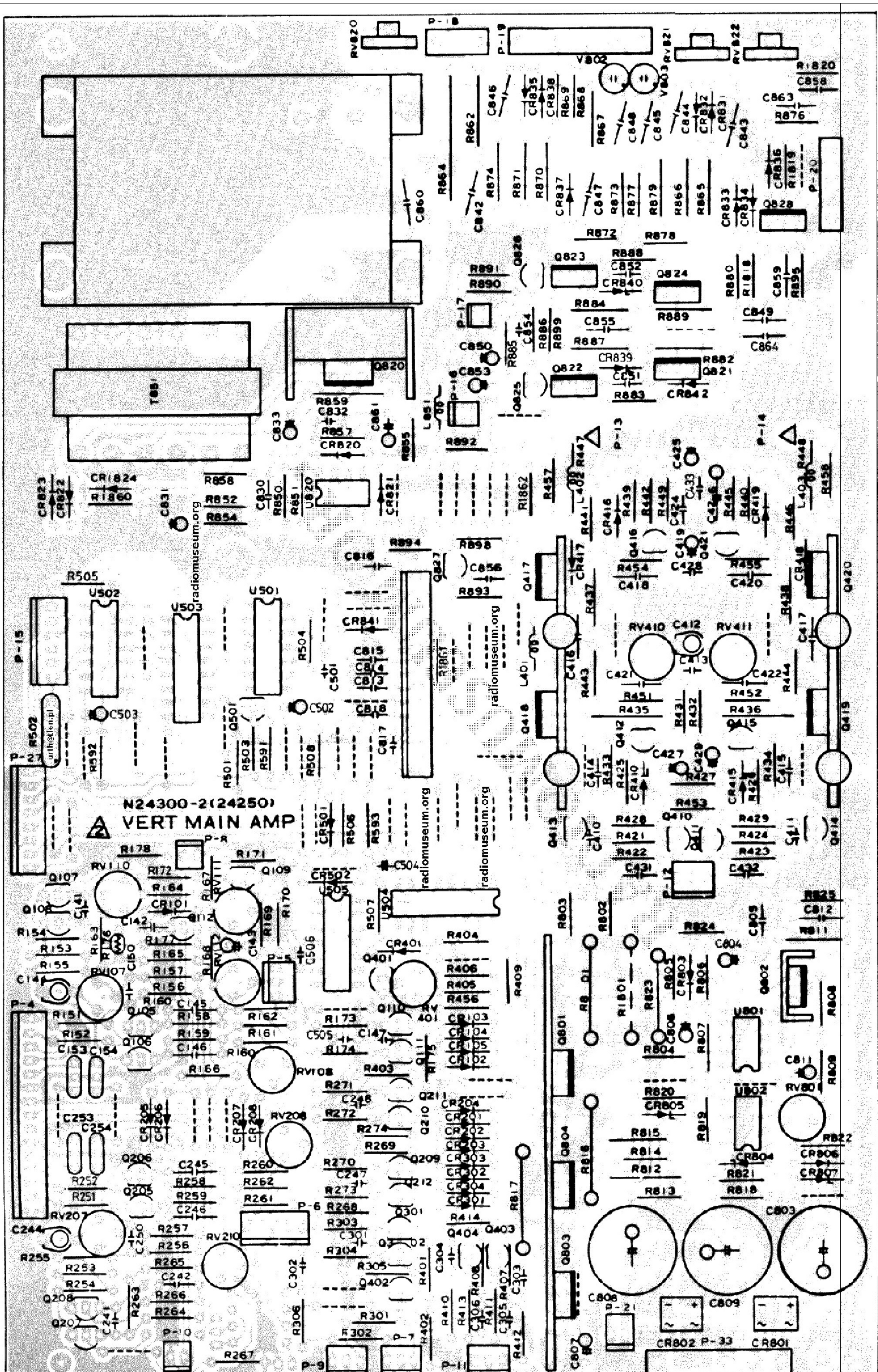
Cal & CRT Control A4 Parts Location Diagram

(Parts Side Veiw)



Vert Preamp A1 Parts Location Diagram

(Parts Side Veiw)


N24300-2(24250)
VERT MAIN AMP
radiomuseum.org
urth@tlen.pl

LOWER PRINTED CIRCUIT BOARDS

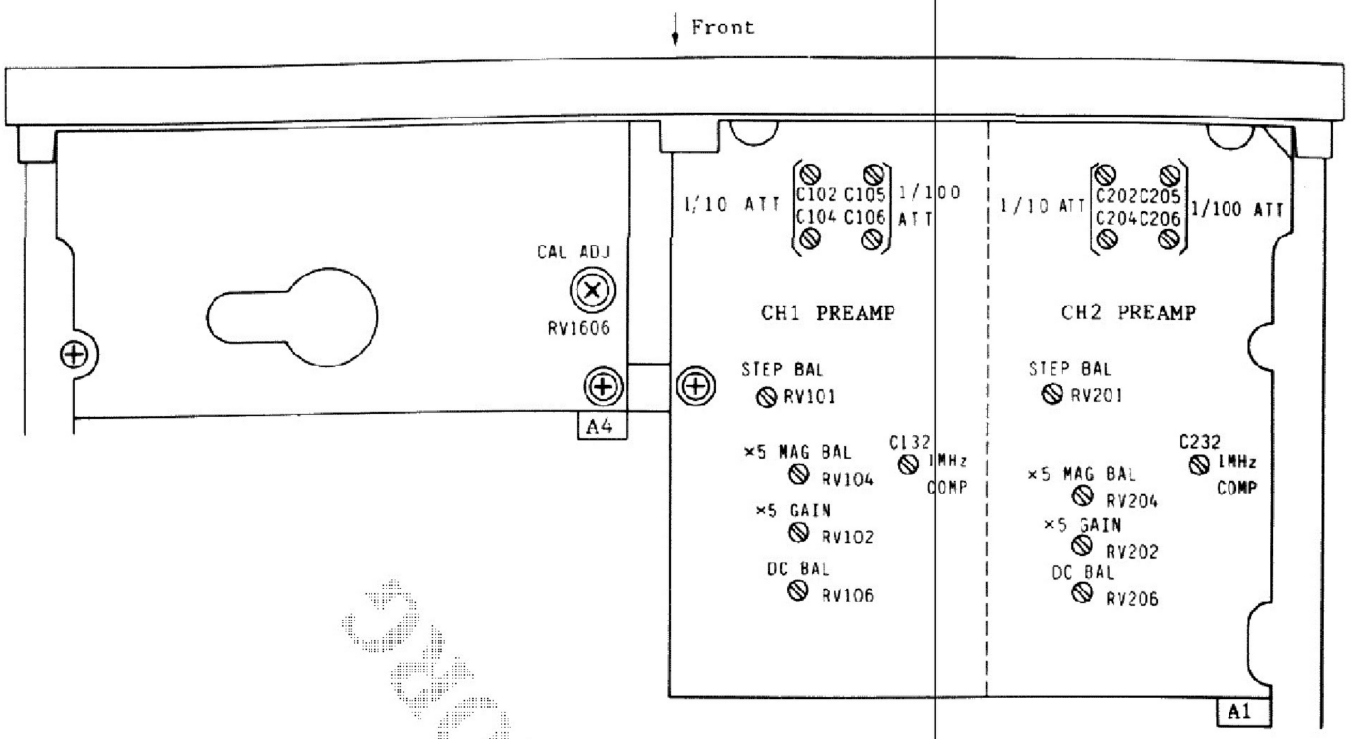


Figure 7-8

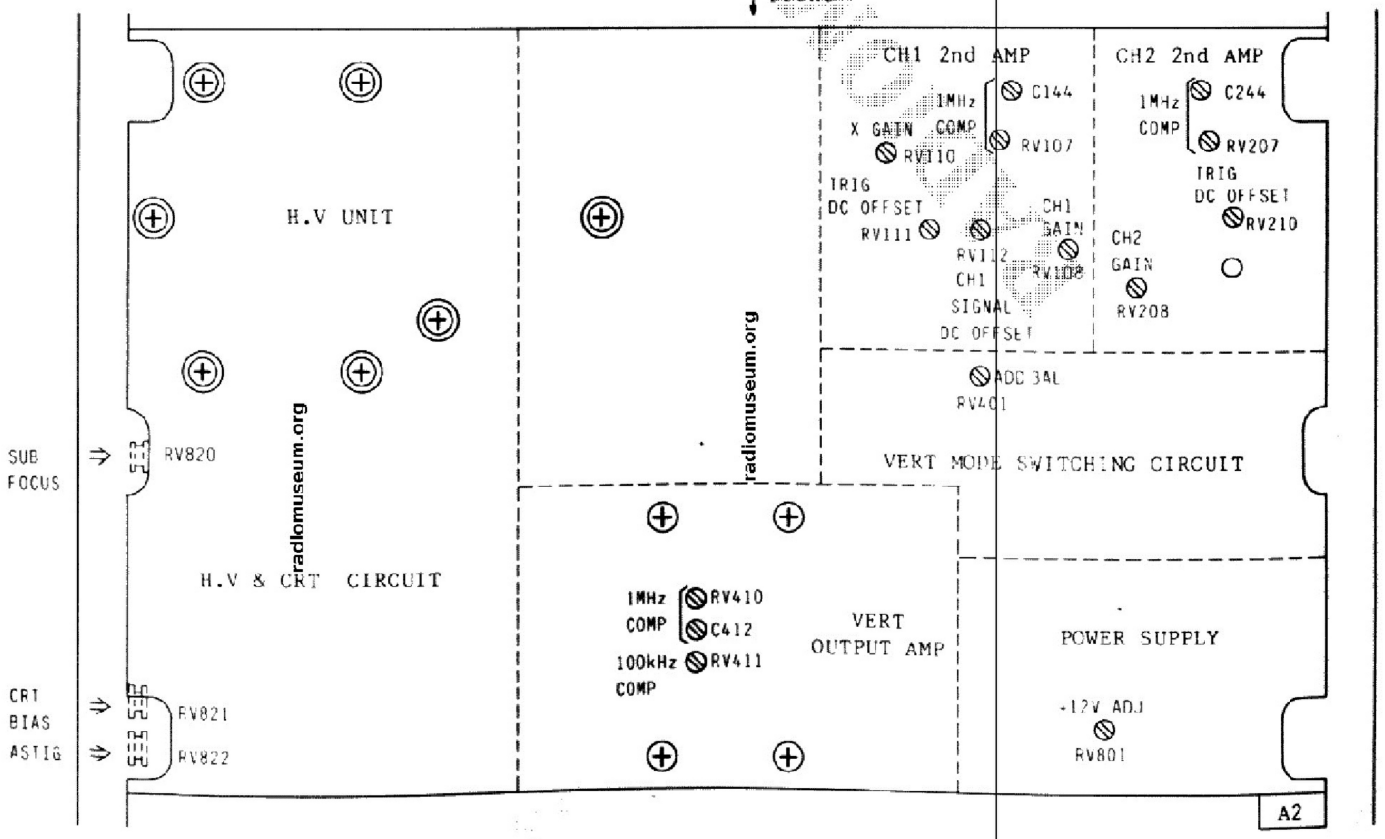
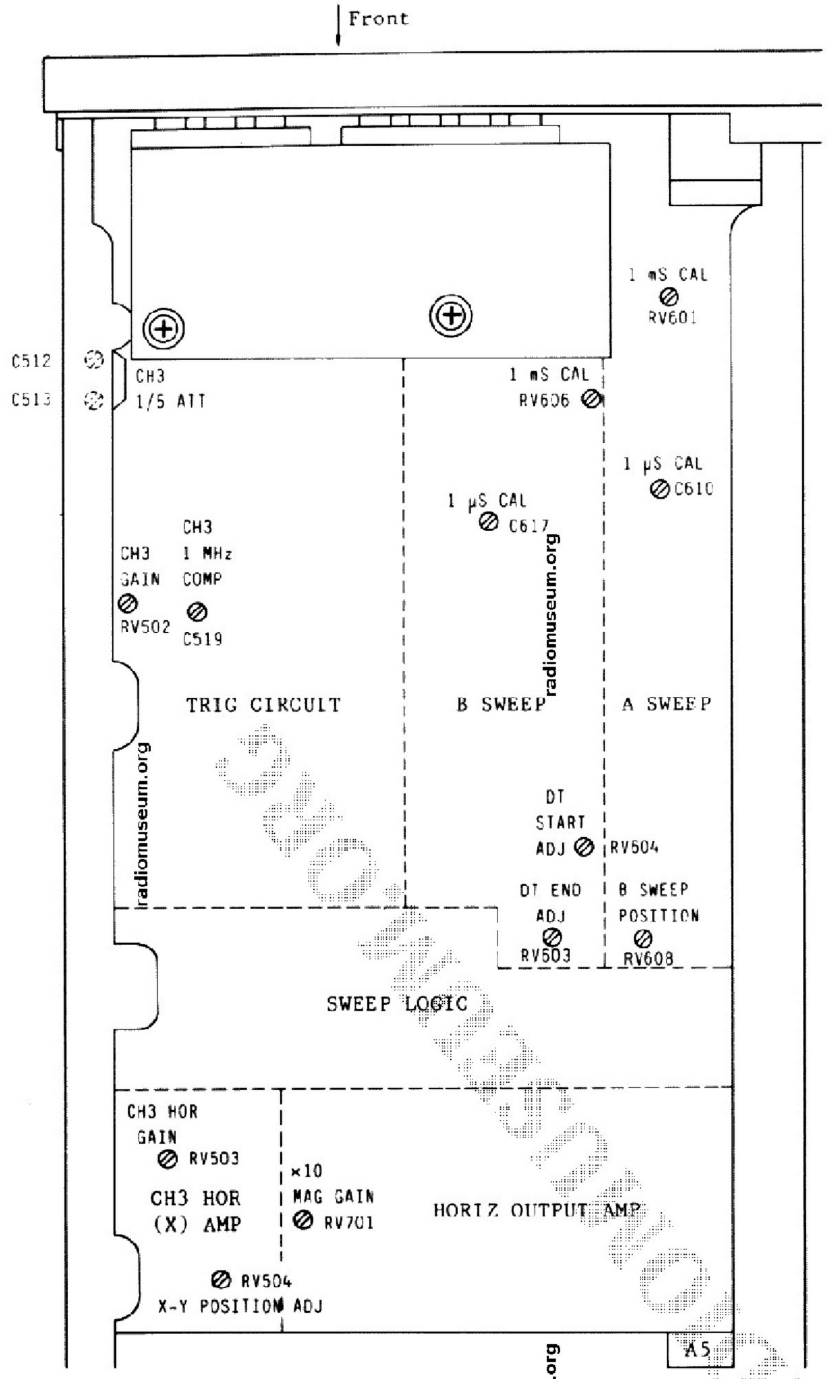
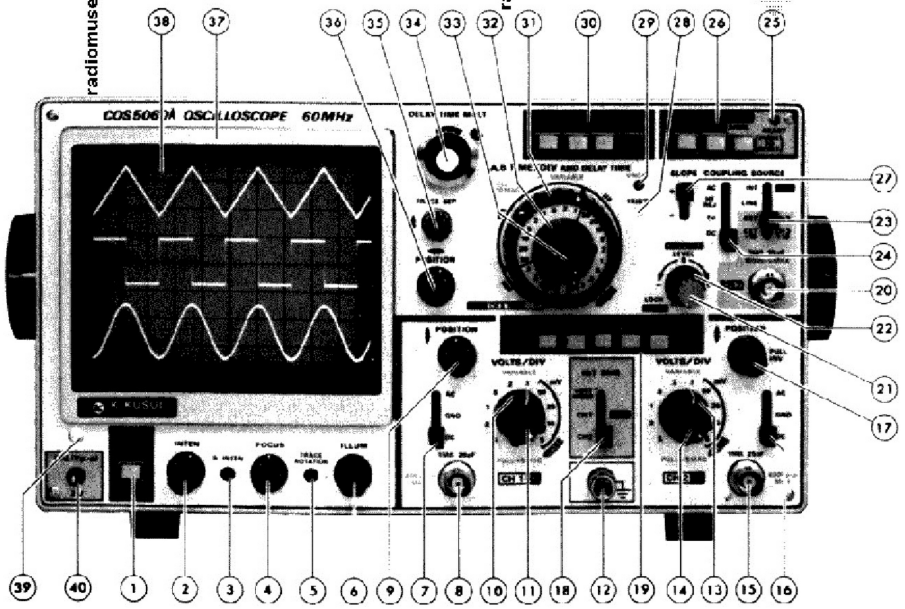


Figure 7-7



UPPER PRINTED CIRCUIT BOARD

Figure 7-9



6. CIRCUIT DESCRIPTION

6.1 General

The overall circuit structure of the oscilloscope is as depicted with a block diagram in Figure 6-1. It is comprised of a vertical deflection circuit for moving the beam spot in the Y-axis direction on the CRT screen, a horizontal deflection circuit for moving the beam spot in the X-axis direction, a CRT circuit for operating the cathode-ray tube, a calibrator circuit for calibrating the instrument probe, and a power supply circuit for supplying powers to the various circuits of the instrument.

The vertical amplifier circuit has two mutually independent preamplifiers (CH1 and CH2), a vertical switching circuit, a delay line, and a vertical output amplifier.

Each of the preamplifiers amplifies or attenuates its input signal of several millivolts to several hundreds volts into a level suitable for handling by the subsequent stages. The conditioned vertical signals are sent to the vertical switching circuit. The trigger signals also are picked off at this stage.

The vertical switching circuit electronically switches the vertical signals received from the CH1 and CH2 preamplifiers and the CH3 signal received from the trigger generator. The switched signal is fed via the delay line circuit to the vertical output amplifier. The trigger signals also are switched and fed as internal trigger signals to the trigger generator.

The vertical output amplifier amplifies the vertical signal, which is received through the delay line circuit, into a level of several volts to several tens volts for vertically deflecting the beam spot on the CRT screen.

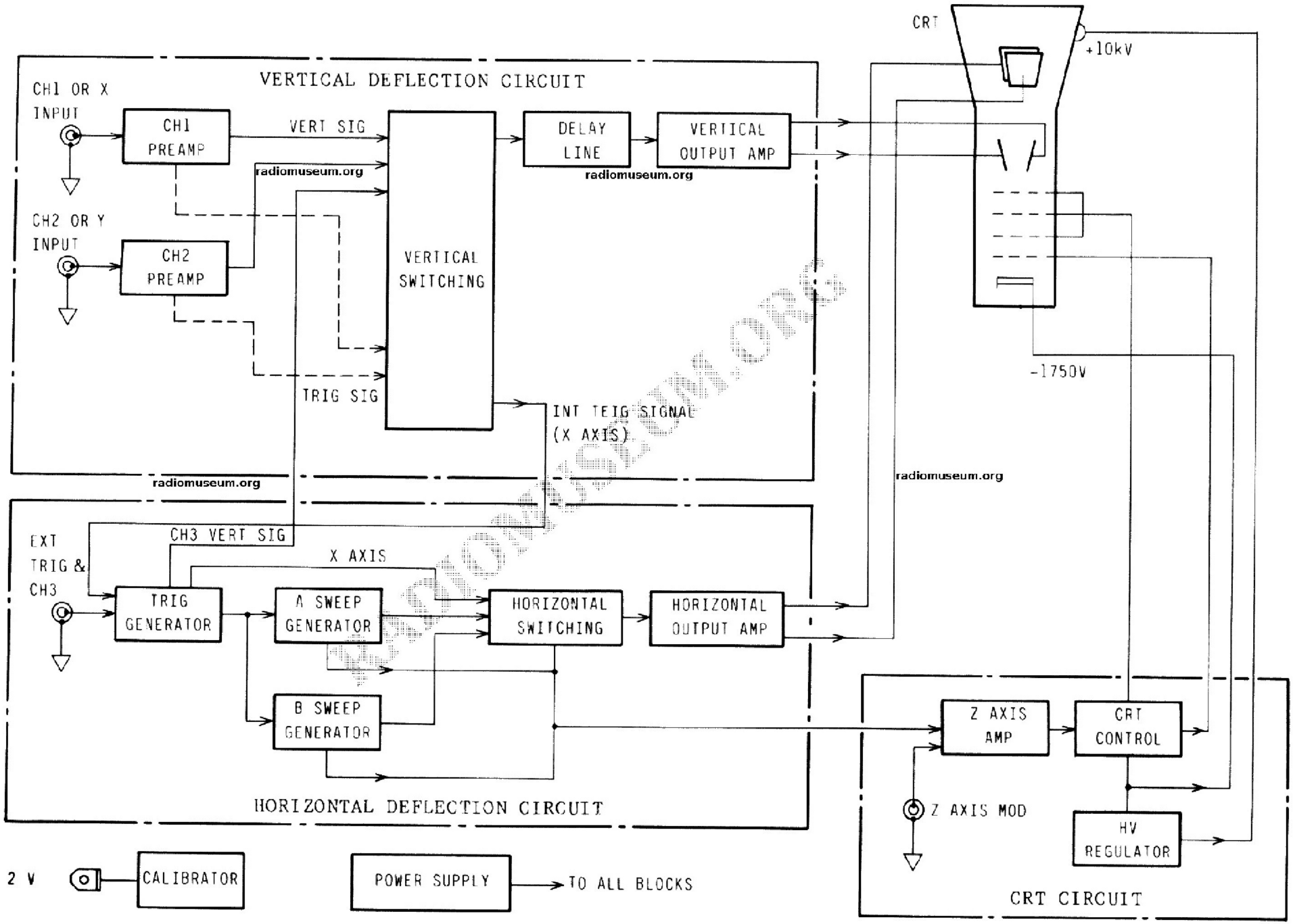

VERTICAL DEFLECTION CIRCUIT
CH1 OR X INPUT
CH1 PREAMP
VERT SIG
DELAY LINE
VERTICAL OUTPUT AMP
CH2 OR Y INPUT
CH2 PREAMP
VERTICAL SWITCHING
TRIG SIG
INT TRIG SIGNAL (X AXIS)
CRT
+10kV
-1750V
EXT TRIG & CH3
CH3 VERT SIG
X AXIS
TRIG GENERATOR
A SWEEP GENERATOR
B SWEEP GENERATOR
HORIZONTAL SWITCHING
HORIZONTAL OUTPUT AMP
HORIZONTAL DEFLECTION CIRCUIT
Z AXIS AMP
CRT CONTROL
Z AXIS MOD
HV REGULATOR
CRT CIRCUIT
2 V
CALIBRATOR
POWER SUPPLY
TO ALL BLOCKS
radiomuseum.org

Figure 6-1

The horizontal deflection circuit has a trigger generator, sweep generator, a horizontal switching circuit, and a horizontal output amplifier.

The trigger generator receives the internal trigger signal from the vertical switching circuit or an external trigger signal from the EXT TRIG (CH3) INPUT terminal and amplifies the signal and generates a trigger pulse signal.

The A sweep generator is driven by the trigger pulse signal of the trigger generator and produces the A sawtooth signal. The sweep generator produces a sawtooth signal even when no trigger pulse is applied to it (the AUTO mode).

The B sweep generator produces the B sawtooth signal, being driven by the delayed sweep start signal produced with respect to the A sawtooth signal when in the continuous delay mode (HOR DISPLAY: B). When in the synchronized delay mode (HOR DISPLAY: B TRIG'D), the B sweep generator generates the B sawtooth signal being driven by the trigger pulse signal of the trigger generator which follows the above delayed sweep start signal.

The horizontal switching circuit electronically switches the sawtooth signals received from the A and B sweep generators and the CH1 & CH3 HOR signal received from the vertical switching circuit when in the X-Y mode of operation, and sends the resultant signal to the horizontal output amplifier.

The horizontal output amplifier amplifies the output signal of the horizontal switching circuit to a level of several volts to several tens volts in order to drive horizontally the beam spot on the CRT screen.

The CRT circuit is comprised of a high voltage generator (the HV regulator) to accelerate the electron beam emitted from the CRT cathode, a Z-axis amplifier to amplify the signal to blank out the return traces, and a CRT control circuit to operate the CRT tube in its optimal state.

The HV regulator provides a -1.8 kV voltage which is applied to the CRT cathode to accelerate the electrons emitted by it and a 10 kV voltage which is used as a post-acceleration voltage to accelerate further the electrons after passing the vertical and horizontal deflection plates.

The Z-axis amplifier amplifies the unblanking signals received from the A and B sweep generators and the trace intensity control signal to a level of several tens volts in order to be applied to the 1st grid (control grid) of the CRT via the CRT circuit.

The CRT circuit provides the various voltages for the CRT electrodes so that the CRT operates in an optimal state, displaying sharply-focussed less-distorted signal waveforms. It also conditions the signals received from the Z-axis amplifier and other circuits into levels suitable for application to the CRT.

6.2 Preamplifiers

The CH1 preamplifier amplifies the signal of the CH1 or X input terminal. The CH2 preamplifier amplifies the signal applied to the CH2 or Y input terminal. A detailed block diagram is shown in Figure 6-2.

- Input coupling switch:

The input coupling switch (S101/S201) selects the input coupling mode for AC, GND, or DC. When the GND state is selected, the preamplifier input is isolated from the input terminal and is grounded so that the base line (0 level) on the CRT screen can be checked.

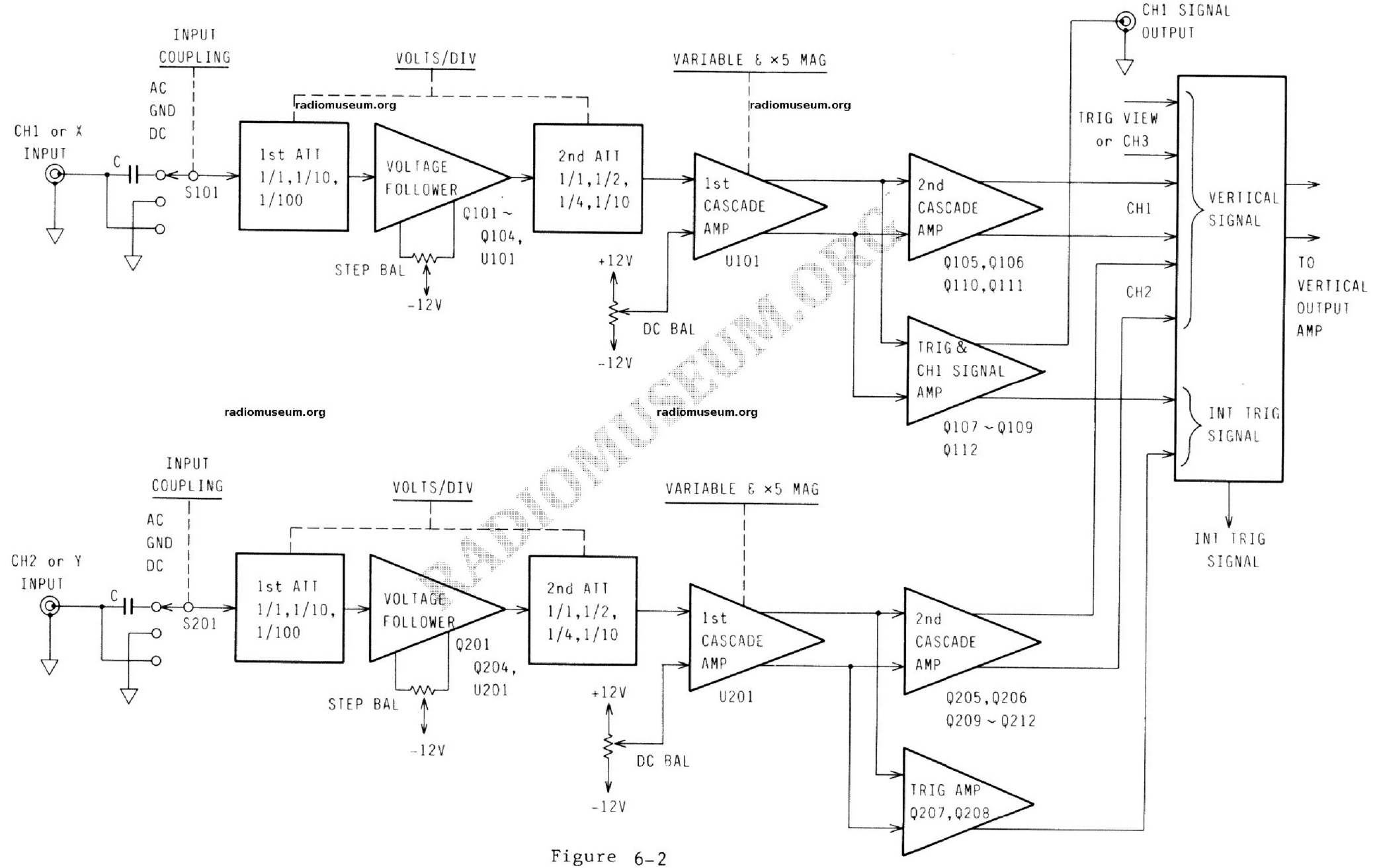


Figure 6-2

o Attenuators:

Each of the CH1 and CH2 attenuator circuits consists of two attenuators: The 1st attenuator for 1/1, 1/10 and 1/100, and the 2nd attenuator for 1/1, 1/2, 1/4 and 1/10. By switching these attenuators with the VOLTS/DIV switch (S102/202), the signal can be attenuated for a total range of 1/1 to 1/1000 in 10 steps.

The 1st attenuator directly attenuates the signal received from the input coupling switch and feeds the attenuated signal to the voltage follower. The 2nd attenuator attenuates the low-impedance output signal of the voltage follower and feeds the attenuated signal to the 1st differential cascade amplifier.

o Impedance converter:

The impedance converter provides with its source follower (Q101/Q201) a high input impedance to prevent the loading effect on the high-impedance attenuator circuit and provides a low output impedance with its emitter follower (CH1 and CH2) to drive the 1st differential cascade amplifier of the next stage. In order to guard against thermal drift, the source follower employs a dual-FET package which houses two thermally-coupled elements for thermal drift compensation and the emitter follower employs two premium-grade thermally-coupled transistors.

o 1st differential cascade amplifier:

The 1st differential cascade amplifier is comprised of an emitter-connected differential current amplifier (U102-1/2, U202-1/2) and a current-to-voltage converter (U102-2/2, U202-2/2) which converts the differential collector output current of the differential current amplifier into a voltage signal. This amplifier also has the VARIABLE circuit for continuously variable adjustment of the sensitivity between two adjoining vertical deflection sensitivity ranges selected by the VOLTS/DIV switch and the ×5MAG switch for magnifying the vertical sensitivity by 5 times to realize the 1 mV/DIV sensitivity.

o VARIABLE circuit:

The VARIABLE circuit continuously-variably adjusts the vertical sensitivity by shunting with potentiometer RV105/RV205 a part of the collector current amplified by U102-1/2 or U202-1/2. Adjustment (attenuation) can be done with a ratio of 1/2.5 or over.

o ×5MAG circuit:

The ×5MAG function is to increase the vertical sensitivity by 5 times by switching the emitter resistor of the 1st differential cascade amplifier.

o 2nd differential cascade amplifier:

The 2nd differential cascade amplifier (Q105, 106, 110, 111, or Q205, 206, 209 - 212) amplifies the output of the 1st differential cascade amplifier to a sufficient level for driving the vertical switching circuit. The grounded-base stage (Q110, 111/Q209 - 212) of this cascade amplifier has a function of preventing the switching signal of the vertical switching circuit from being returned to the preceding stage and mixed into the trigger signal or the signal of the CH1 signal output amplifier. For the CH2 signal, this amplifier also has a function of inverting its polarity. This polarity inverting function is accomplished by switching with the INV switch the base grounding stages of Q209/210 and Q211/212 to which the collector currents which have been current-amplified by Q205 and Q206 are fed in a crossing manner.

Different from the case of the 1st differential cascade amplifier, the output signal of the 2nd differential cascade amplifier is fed directly in the form of the current signal to the diode gate of the vertical switching circuit. The current signal for vertical positioning of the trace on the CRT screen is added to the output current signal of the 2nd differential cascade amplifier, being controlled by potentiometer RV109/209 of the positioning circuit.

o Trigger signal amplifier (& CH1 signal output amplifier):

This circuit amplifies with its Q107, 108/Q207, 208 the signal picked off from the 2nd differential amplifier, and converts with its Q109 the collector output of Q107 into a low-impedance CH1 output signal which is fed to J-8C. The collector output signal of Q108/Q208 is fed as a trigger signal to the internal trigger switching circuit.

6.3 Vertical Switching Circuit

The vertical switching circuit is comprised of a vertical signal switching circuit (diode gate circuit) which electronically switches the vertical signals received from the CH1 and CH2 preamplifiers and the CH3 signal received from the TRIG generator, an internal trigger signal switching circuit which electronically switches the trigger signals, and a switching logic circuit which controls these switching circuits.

The vertical signal switching circuit is, as shown in Figure 6-3, comprised of a diode gate circuit, an ADD BAL circuit, and a switching buffer circuit which receives the signal from the diode gate circuit.

o Diode gate circuit:

The diode gate circuit (CR102 - 105, CR201 - 204, CR301 - 304) selects the CH1 - CH3 signals being controlled by the signal of the switching logic circuit according to the mode selected by the VERT MODE switch (S501).

For example, when the VERT MODE switch is set at CH1, the CH1 control signal becomes the Hi state, and the CH2 and CH3 control signals become the Lo state. Consequently the output signal of the CH1 preamplifier is fed through CR104 and CR105 to the switching buffer circuit consisting of Q403 and Q404. The signals of the other channels are fed through respective diodes CR202/203 and CR302/303 to the control circuit. Thus, the signal of CH1 alone is fed to the switching buffer circuit and the signals of the remaining channels are blocked.

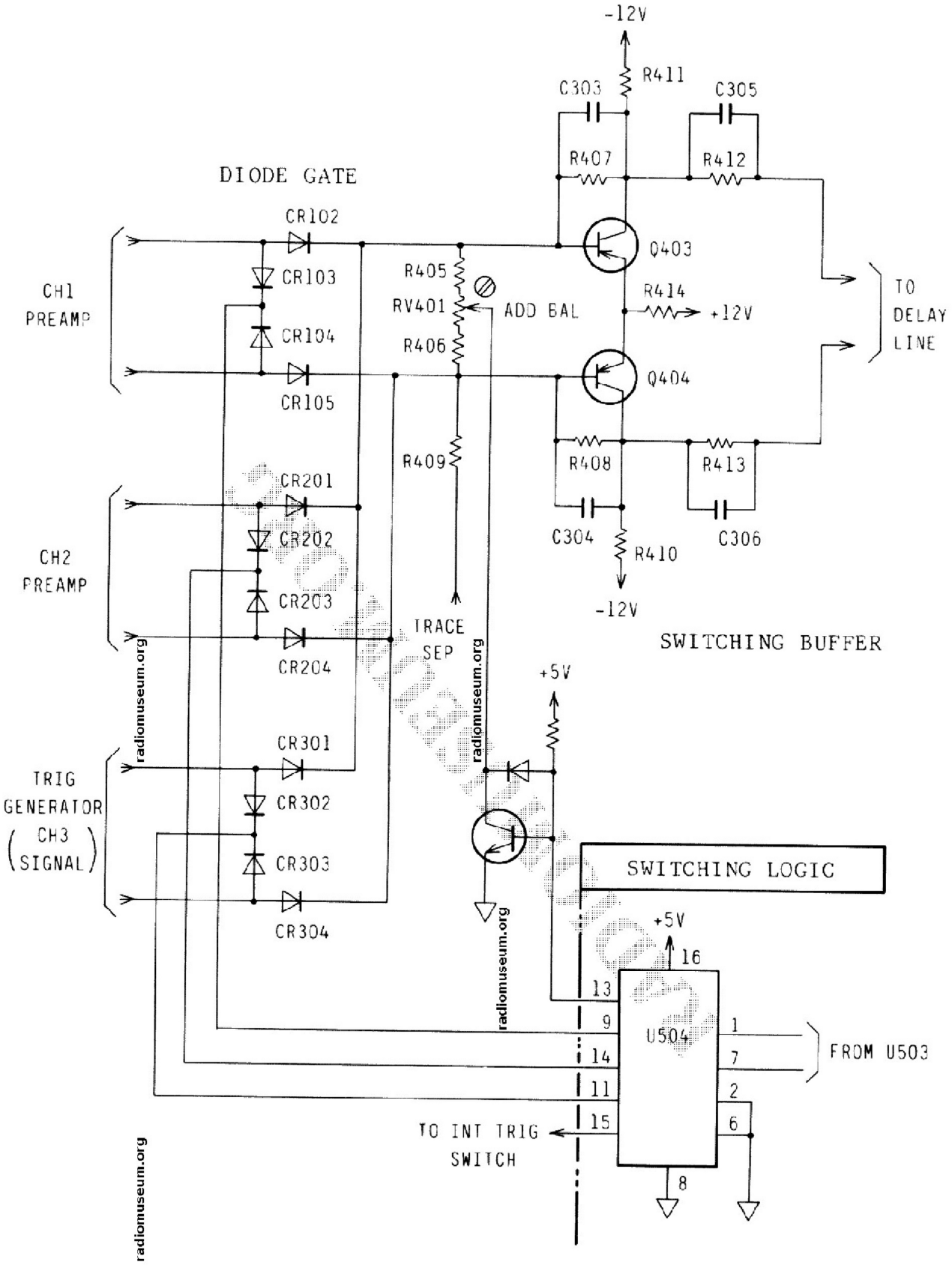


Figure 6-3 Vertical switching circuit

o ADD BAL circuit:

When the ADD mode is selected by the VERT MODE switch, the control signals of both CH1 and CH2 become the Hi state, the signals of the CH1 and CH2 preamplifiers are fed through CR104/105 and CR201/204 to the switching buffer circuit, and the two signals are fed as their sum signal to the output circuit. The function of the ADD BAL circuit is to compensate for the DC balance shift caused by the above addition operation, with its ADD BAL control (semi-fixed potentiometer RV401).

o Internal trigger signal switching circuit:

The internal trigger signal switching circuit directly controls, with the control signals from the switching logic circuit, the diode gate circuit (CR205 - 208) which is similar to the vertical signal switching circuit. The trigger signal which has passed the diode gate circuit is delivered as the internal trigger signal via connector P-10.

o Switching logic circuit:

The switching logic circuit is comprised of a vertical switching logic circuit which controls the vertical signal switching circuit and an internal trigger switching logic circuit which controls the internal trigger signal switching circuit.

The vertical switching logic circuit is comprised of a ring counter which is consisting of two flip-flops (U503-1/2, 2/2) with preset/clear terminals and a code converter (U504) which receives the ring counter output and generates control signals for individual channels. Switching can be done for any combination of channels by turning on and off the preset/reset terminals of the ring counter. The code-converted control signal is fed to the internal trigger switching logic circuit.

The internal trigger switching logic circuit controls the internal trigger switching circuit by switching with IC U505 the control signal selected by the INT TRIG switch (S502) and the control signal received from the vertical switching logic circuit. This relationship is shown in the following table.

MODE / INT TRIG	CH1	ADD	CH2	TRIG VIEW / CH3
CH1	Triggered by CH1			
CH2	Triggered by CH2			
VERT MODE	Trig'd by CH1	Trig'd by CH1	Trig'd by CH2	Trig'd by CH1

*: The triggering functions of VERT MODE are effective only when in a single-channel display or in a multiple-channel display in the ALT mode. They remain idle when in the CHOP mode.

6.4 Delay Line Circuit

The vertical signal which has passed the diode gate circuit is amplified by the switching buffer circuit (Q403, Q404). The switching buffer circuit drives the delay line, with a matched output impedance.

The delay line is used to prevent the trigger point of the signal from being lost from being displayed on the screen due to time lag in the horizontal deflection circuits or the Z-axis amplifier circuits. For the delay line, this oscilloscope employs a delay cable which provides a delay time of approximately 100 nanoseconds. The vertical signal which has passed the delay line is fed to the vertical output amplifier.

6.5 Vertical Output Amplifier

The vertical output amplifier is comprised of a delay line receiver which receives the output signal of the delay line with a matched impedance, and a final amplifier which drives the vertical deflection plates of the CRT.

o Delay line receiver circuit:

The delay line receiver circuit (Q410, 411) is a low input impedance negative feedback amplifier which, with its input resistors R422 and R423, provides impedance matching with the characteristic impedance (Zo ≒ 186 ohms) of the delay line.

o Final amplifier:

The final amplifier boosts the signal to a level sufficient for driving the vertical deflection plates of the CRT. It is comprised of a pair of feedback-type SEPP amplifiers.

Transistors Q412, 413/Q414, 415 current-amplify the signal to a level sufficient for driving transistors Q417, 418/Q419, 420. The signal which has been voltage-amplified by transistors Q417, 418/Q419, 420 is returned to the input circuit through the negative feedback circuit (R435/R436). The gain in this case is as follows:

$$Av = \frac{R435}{R428} \qquad Av' = \frac{R436}{R429}$$

Transistors Q416/Q421 are for the dynamic bias circuit which controls the bias current with respect to the repetition frequency of the signal in order to economize current consumption.

6.6 Trigger Generator

The trigger generator is comprised of a trigger pulse generator circuit which produces a trigger pulse signal for driving the sweep generator and an AUTO circuit which produces a free-run signal for automatic sweep operation when the trigger signal is asynchronized or no trigger signal is applied.

The trigger pulse generator circuit of the trigger generator is comprised of a source switch which selects a trigger signal source, a coupling switch which selects a coupling mode in conformity with the nature of the trigger signal source, an impedance converter circuit which converts the high-impedance trigger source signal into a low-impedance signal with which to drive the level comparator circuit which controls the start point (triggered point) of the signal waveform displayed on the CRT screen, a TV synchronization separator circuit which picks off the synchronization signal from the TV video signal, and Schmitt trigger circuits which convert the output signals of the level comparator circuit and TV synchronization signal separator circuit into TTL level signals.

o Source switch:

The source switch (S502) selects the internal trigger signal fed from Q510, the line trigger signal fed from R585, the external trigger signal fed directly from J-61C, or the signal fed from J61C through the 1/5 attenuator in order to be converted into the EXT ÷ 5 TRIG signal. The selected signal is fed to the coupling switch.

o Coupling switch:

The coupling switch (S503) selects the coupling mode: It selects the DC mode for direct coupling of the signal fed from S502, the AC mode for discarding the DC component, or the HF REJ mode for coupling via a low-pass filter. Switch S503 selects ON or OFF of the TV synchronization signal separator circuit which facilitates observation of a TV video signal.

o Impedance converter:

The impedance converter is a temperature-compensated-type cathode follower (Q512) with dual FET's. It converts the trigger signal selected by the source switch and coupling switch into a low-impedance signal. The impedance is lowered further by the emitter follower of U510 and then the signal is fed to drive the level comparator circuit.

It also delivers the TRIG VIEW and CH3 signals from its U510 Pins Nos. 8 and 11.

o Level comparator:

The level comparator is a differential cascade amplifier (U510, Q513, Q514) which adjusts the rise up portion (or the fall down portion) of the comparator output signal by applying to U510 Pin No. 9 of the current amplifier stage the trigger source signal from the impedance converter circuit and adding to U510 Pin No. 6 the comparator level signal from the LEVEL control potentiometer (RV501-1). In this case, if switch S503 which is linked to the LEVEL control potentiometer is locked, the comparator level signal is applied to U501 Pin No. 6 from the level lock circuit and the trigger point is fixed at the center amplitude of the trigger source signal.

The level lock circuit amplifies with its error amplifier (U511) the error signal detected by Q515 and Q516, and feeds back the signal so that the center level of the comparator output signal becomes the Schmitt level of the Schmitt trigger circuit.

It also selects a slope by switching the polarity of the output signal of the cascade amplifier (U501) with the diode switch circuit.

The output signal of the cascade amplifier is fed via the buffer amplifier which is used also as a TV synchronization signal separator circuit.

o Buffer amplifier/TV synchronization signal separator circuit:

This circuit operates either as a buffer amplifier or as a TV synchronization signal separator circuit, being selected by the transistor switching circuit (Q517, 518).

When Q517 is on and Q518 is off, the circuit operates as a buffer amplifier and amplifies the output signal of the level comparator to a level sufficient for driving the Schmitt circuit of the next stage.

When Q517 is off and Q518 is on, the circuit operates as a TV synchronization signal separator circuit and picks off the TV-H synchronization signal, which is pulsewidth-detected into a TV-V synchronization signal by the Schmitt circuit of the next stage.

o TRIG Schmitt circuit:

The TRIG Schmitt circuit is a conventional one which generates a hysteresis voltage by applying a beedback signal with R567 to the two stages of NAND gates of U512. The output of the Schmitt circuit drives the A and B SWEEP generators and AUTO circuit.

o AUTO circuit:

The AUTO circuit is comprised of a uni-junction transistor (UJT) circuitry made up by connecting mutually the bases and collectors of a PNP transistor (Q521) and an NPN transistor (Q522). This circuit converts the high-speed pulse output signal of the Schmitt circuit into a DC signal, which is conditioned for waveform-shaping by the gate circuit (U513) to drive the A sweep generator and the TRIG'D LED lamp.

6.7 A and B Sweep Generators

The A sweep generator produces the sawtooth signal for the main sweep (A sweep) of this oscilloscope. The B sweep generator produces the sawtooth signal for magnification in the time axis direction the waveform displayed on the main sweep or for display with a certain time delay (delayed sweep or B sweep).

The A sweep generator consists of the A sweep gate circuit which receives the trigger signal from the trigger generator and produces the sweep gate signal for starting sweeps, the sweep start comparator which maintains stably the sweep start point, the A sawtooth sweep generator which produces a sawtooth wave in conformity with the time constant selected by the TIME/DIV switch, the sweep length circuit which controls the length of sweeps, the hold off circuit which controls the sweep return period and pause period, and the A sweep gate enable circuit which controls the sweep gate circuit in conformity with the AUTO, NORM or SINGLE mode as selected by the MODE switch for the signals of the above control circuits.

o A sweep gate:

The A sweep gate circuit employs a flip-flop TTL IC (U602-1/2) with preset/clear function. The trigger pulse of the trigger generator is applied to the CLOCK (Pin No. 1) terminal, the enable signal of the A sweep gate enable circuit to the CLEAR (Pin No. 15) terminal, and the enable signal and AUTO signal of the AUTO circuit to the PRESET (Pin No. 4) terminal through the NOR gate circuit. The Q (Pin No. 5) terminal output is applied as the unblanking signal to the Z-axis amplifier and the $\overline{Q}$ (Pin No. 6) terminal output is fed to the sweep start comparator circuit and becomes the A sweep gate signal. Even when no trigger pulse signal is applied to the CLOCK terminal, the $\overline{Q}$ output can be made the low state with the AUTO signal of the PRESET terminal so that the A sweep gate signal is generated and the circuit operates in the free-run mode.

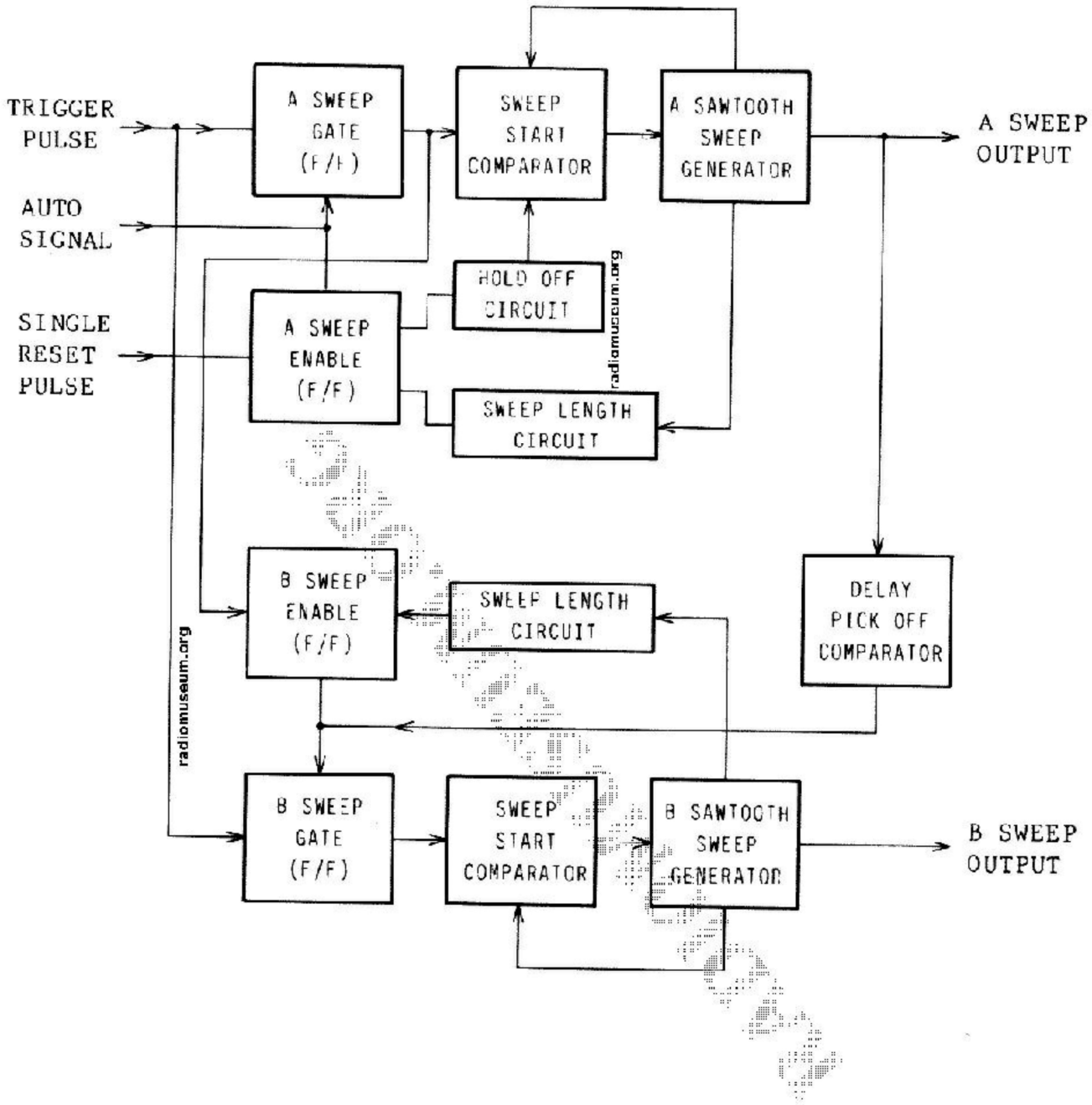

TRIGGER PULSE
AUTO SIGNAL
SINGLE RESET PULSE
A SWEEP GATE (F/F)
SWEEP START COMPARATOR
A SAWTOOTH SWEEP GENERATOR
A SWEEP OUTPUT
HOLD OFF CIRCUIT
A SWEEP ENABLE (F/F)
SWEEP LENGTH CIRCUIT
B SWEEP ENABLE (F/F)
SWEEP LENGTH CIRCUIT
DELAY PICK OFF COMPARATOR
B SWEEP GATE (F/F)
SWEEP START COMPARATOR
B SAWTOOTH SWEEP GENERATOR
B SWEEP OUTPUT
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Figure 6-4

o Sweep start comparator:

The sweep start comparator (Q601, 602) is a differential amplifier which lets the sweep gate signal pass and maintains constant the sweep start level. A start reference level identical with the B sweep start level is applied to one of the inputs, the Miller integrator output signal is applied to the other input, and the difference between the two signals is compensated for.

o A sawtooth generator:

The A sawtooth generator is comprised of a gate transistor amplifier, a Miller integrator, an integration time constant switching circuit, and a TIME/DIV switch which controls the switching circuit. The gate transistor amplifier (Q604) controls the Miller integrator circuit in such manner that the start level control signal and sweep gate signal of the sweep start comparator do not affect the integration time constant. The Miller integrator (Q606, 607) produces a sawtooth signal with the time constant selected by the integration time constant selector circuit. The integration time constant selector circuit selects integration capacitor C609/C611 with Q605. For integration current, resistor array R671 is directly selected by the TIME/DIV switch (S604-2).

o Sweep length circuit:

The sweep length circuit divides with resistors R620 and R621, and shapes the waveform with Q612 to obtain a sweep length signal.

o Holdoff circuit:

The holdoff circuit generates a holdoff (pause) time signal proportional to the sweep time by producing a triangular wave with an integrator circuit and making use of the rise time of the triangular wave. The integrator, with its Q610, selects the time constant in accordance with the integration output voltage in order to cover a wide time range. The output signal of the integrator circuit is shaped by Q611 into a holdoff signal.

o A sweep gate enable circuit:

The A sweep gate enable circuit employs the flip-flop IC (U602-2/2) which makes up a pair with the A sweep gate circuit. The holdoff signal is applied to the PRESET (Pin No. 10) terminal, the length signal is applied to the CLEAR (Pin No. 14) terminal, and the enable signal is delivered from the Q (Pin No. 9) terminal. This enable signal presets or clears the A sweep gate circuit. When in the NORM sweep mode, the output signal of the AUTO circuit is blocked and, if no trigger signal is applied, the circuit is in the ready state. When in the SINGLE sweep mode, the holdoff circuit remains idle and a one-shot sweep is effected by the reset signal applied from the CLOCK (Pin No. 13) terminal.

The basic structure of the B sweep generator is identical with that of the A sweep generator. It consists of the B sweep gate, sweep start comparator, B sawtooth generator, sweep length circuit, B sweep enable circuit, and delay pickoff comparator. The B sweep generator requires no holdoff circuit because it operates only during the period the A sweep generator is in the sweep operation. Instead of the holdoff signal, the A sweep gate signal sets the B sweep enable circuit to the enable state.

o Delay pickoff comparator:

The delay pickoff comparator (Q613 - 615) employs a dual FET (Q615) to obtain a certain time relationship as set by the delay time multiplication potentiometer (RV605) with respect to the A sweep signal. The comparator compares the A sweep output signal (sawtooth waveform) with the voltage set by RV605, generates a delayed sweep start signal, and sets the B sweep gate circuit to start the B sweep signal. When in the B TRIG'D mode, the B sweep gate circuit is not set directly with this delayed sweep start signal but the PRESET (Pin No. 4) terminal is set to the high state and the B sweep signal is started as driven by the trigger pulse of the trigger generator.

6.8 Horizontal Switching Circuit

The horizontal switching circuit is comprised of a switching buffer circuit which prevents switching distortion from being sent to the sweep circuit of the preceding stage, a display switching circuit which electronically switches the A and B sweep signals and CH1 HOR (X) signal, and a display logic circuit to control these circuits.

- Switching buffer circuit:

The switching buffer circuit is of a grounded-base-type amplifier. Transistor Q608 is for buffer-amplification of the A sweep signal, transistor Q626 for the B sweep signal.

- Display switching circuit:

The display switching circuit, with its analog signal multiplexer IC (U607), selects the A and B sweep signals and CH1 HOR (X) signal.

- Display switching logic circuit:

The display switching logic circuit, with its flip-flop (U606-1/2) which has a preset/clear terminal, controls the display switching circuit in conformity with the operation mode selected by the HOR DISPLAY switch (S601). With its another flip-flop (U606-2/2), it generates the alternate switching pulse signal for the vertical axis circuits.

6.9 Horizontal Output Amplifier

The horizontal output amplifier consists of a drive amplifier which selects between NORM and ×10 MAG mode for the horizontal signal received from the horizontal switching circuit and drives the output amplifier, and an output amplifier which drives the horizontal deflection plates of the CRT.

o Drive amplifier:

The drive amplifier (Q701 - 704) converts the horizontal signal received from the horizontal switching circuit into a differential signal, with which to drive the output amplifier. With Q701 and 702, gain of the differential amplifier can be multiplied by a factor of 10 for the ×10 MAG function.

o Output amplifier:

The output amplifier (Q705 - 712) is comprised of feedback-type SEPP amplifiers symmetrical for right and left which provide sufficient speed and output voltage for driving the horizontal deflection plates of the CRT. The signal current-amplified by Q705/Q706 is converted into a voltage signal by Q707 - Q712 to obtain a sufficiently high gain and a sufficiently low output impedance. By means of negative feedback resistor R720/R721 a stable gain and wide and flat frequency response are attained.

6.10 Z-axis Amplifier

The Z-axis amplifier is comprised of an input circuit and an output amplifier. The input circuit merges the unblanking signals of the A and B sweep generators, the external intensity modulation signal applied through the Z-axis input terminal, the B intensity control signal, and the overall intensity control signal. The output amplifier amplifies the merged signal into a sufficient level for driving the G1 grid of CRT.

o Input circuit:

The input circuit merges the unblanking signals of the A and B sweep generators, the chopped blanking signal, the external intensity modulation signal applied via the X-axis input terminal, and the overall intensity control signal. The resultant compound signal is fed to the output amplifier.

o Output amplifier:

The output amplifier amplifies the above compound signal to several tens volts. It is of a feedback-type SRPP circuit (Q821, 822, 825). This amplifier also generates (with its Q823, 824, 826) a linear focus signal which is in the inverted phase of the unblanking signal. The amplified unblanking output signal and linear focus signal are fed to the G1 and P1 of the cathode-ray tube through the CRT circuit to drive the intensity and focus of the displayed waveform.

6.11 CRT Control Circuit

The CRT control circuit is comprised of a DC regeneration circuit which converts the linear focus signal and the unblanking output signal of the Z-axis amplifier into the operating-voltage signals of the CRT in order to be applied to the focus electrode and G1 electrode of the CRT, semi-fixed potentiometers ASTIG (RV822), GEOMETRY and SUB-FOCUS (RV820), a trace rotation circuit for adjusting the trace direction in parallel with the horizontal graticule lines, and an illumination circuit for illuminating the graticule.

o DC regeneration circuit:

The DC regeneration circuit converts the linear focus signal and unblanking signal of several tens to several hundreds volts into AC signals with the switching signal of the DC-DC converter circuit, and then converts them back into DC signals with respects to the cathode voltage and focus reference voltage of the sub-focus potentiometer in order to provide a focus signal and an unblanking signal of the operating voltages of the CRT.

6.12 HV Regulator (High Voltage Generator)

The high voltage generator produces an acceleration voltage (-1750 V) applied to the CRT cathode and a post-acceleration voltage (approximately +10 kV) applied to the CRT anode to accelerate the electrons beam which have passed the X and Y deflection plates and mesh electrode. The circuitry is a

DC-DC converter with blocking oscillator (Q820), with resonance of the secondary coil winding. The high voltage of approximately 3600 Vp-p (frequency approximately 30 kHz) generated by the blocking oscillator is 6-times voltage-multiplication rectified by a Cockcroft circuit into a positive voltage of approximately 18 kV and it is half-wave rectified into a negative voltage of -1750 V.

This DC-DC converter feeds the negative voltage of approximately 1800 V via a high resistance circuit (R862, R864) to the control circuit (U820) to obtain a stabilized acceleration voltage. It also is fed through a capacitor-coupling circuit to the DC regeneration circuit in order to be used as the switching signal.

6.13 Power Supply Circuit

The power supply circuit steps up or down with its power transformer the AC line voltage into various voltages and rectifies them to DC supply voltages for the various circuits of the oscilloscope. The primary winding of the power transformer is of a split type, in order that the oscilloscope can be operated on various AC line voltages by connecting the transformer taps in series or parallel as required by means of the line voltage selector plug (P-47). Regarding the secondary circuit, the transformer has one 6.3 V winding for the CRT heater and two windings of different voltages for different circuits of the CRT. The AC voltages of the two windings are rectifies and supplied as non-regulated +16 V power and regulated +145 V, +12 V, +5 V, and -12 V powers.

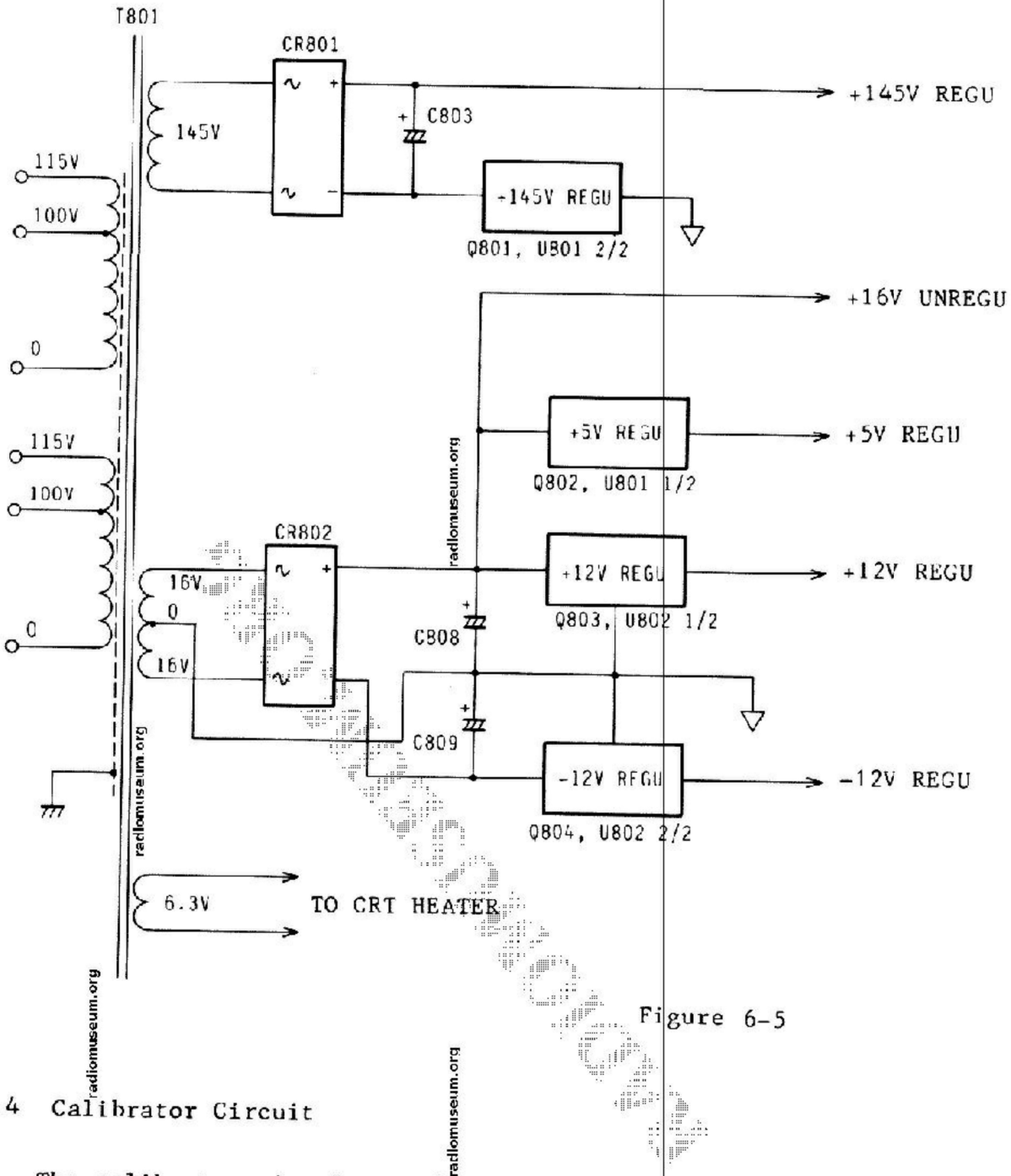

Figure 6-5

6.14 Calibrator Circuit

The calibrator circuit provides square-wave calibration voltage signal of 2 Vp-p which is used for calibration of the probe and the amplifiers when they are operated in the non-calibrated mode. The voltage accuracy of the calibration signals is 2% or better. The calibration signal is produced by generating a signal with the multivibrator of CMOS IC (U1601 1/4, 2/4), shaping the waveform with the Schmitt circuit of CMOS IC (U1601 3/4, 4/4), and dividing the voltage signal with resistors.